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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HARRELL, ROBERT B	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 11/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/005,706	SCHINAZI, STEPHANE	
	Examiner	Art Unit	
	Robert B. Harrell	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-21 and 23-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-21 and 23-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *see attached Office Action*.

1. Claims 15-21 and 23-26 remain presented for examination.

2. The applicant should always use this period for response to thoroughly and very closely proof read and review the whole of the application for correct correlation between reference numerals in the textual portion of the Specification and Drawings along with any minor spelling errors, general typographical errors, accuracy, assurance of proper use for Trademarks ™, and other legal symbols ®, where required, and clarity of meaning in the Specification, Drawings, and specifically the claims (i.e., provide proper antecedent basis for "the" and "said" within each claim). Minor typographical errors could render a Patent unenforceable and so the applicant is strongly encouraged to aid in this endeavor.

3. Prior to addressing the grounds of the rejections below, should this application ever be the subject of public review by third parties not so versed with the technology (i.e., access to IFW through Public PAIR (as found on http://portal.uspto.gov/external/portal/pair)), this Office action will usually refer an applicant's attention to relevant and helpful elements, figures, and/or text upon which the Office action relies to support the position taken. Thus, the following citations are neither all-inclusive nor all-exclusive in nature as the whole of the reference is cited and relied upon in this action as part of the substantial evidence of record. Also, no temporal order was claimed for the acts and/or functions.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this action:

A person shall be entitled to a patent unless –

(e) the invention was described in — (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language;

5. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this office action:

a) a patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claims 15-21 and 23-26 are rejected under 35 U.S.C. 102 (e)*** as being anticipated by Narasimhan et al. (United States Patent Number: US 6,446,192 B1).

7. ***Claims 15-21 and 23-26 are rejected under 35 U.S.C. 103 (a)*** as being obvious by Narasimhan et al. (United States Patent Number: US 6,446,192 B1).

8. The rejections, and grounds for rejections, under 35 U.S.C. 102(e) as presented in examiner's prior Office Action mailed 05 May 2006, are hereby maintained and incorporated in this Office Action by reference.

9. The rejections, and grounds for rejections, under 35 U.S.C. 103(a) as presented in examiner's prior Office Action mailed 05 May 2006, are hereby maintained and incorporated in this Office Action by reference.

10. The applicant argued the rejection under 35 U.S.C. 102(e) and the rejection under 35 U.S.C. 103, in his 08 September 2006 response, by stating in substance that:

a) claim 15 recites the joint integration of a protocol array, a signal processing program, and a supervisory layer software in a single DSP. The applicant respectfully submits that the '192 patent fails to disclose, either explicitly or implicitly, that the program implementing Internet functions (i.e., the protocol array) is loaded in the memory of a DSP. In particular, the SMTP, FTP and HTTP routines of Fig. 2 of the ' 192 patent are stored in the Network interface chip 36. This is not a DSP as specifically recited in Claim 15. As noted in the '192 patent at column 6, lines 14-21, the device control circuitry 38, which may include a DSP according to line 21, has "little or no networking capability." Furthermore, the '192 patent in Fig. 12 discloses a UART (Universal Asynchronous Receiver/Transmitter) for connecting chip 36 to a modem. Thus, chip 36 cannot be considered to be a modem chip inasmuch as it does not comprise modem functionalities. ***However***, as indicated in the citation to 206 USPQ 499 in subparagraph (d) below, the matter of integration is not a novelty point but rather an anticipated matter of system construction for the benefits as so indicate below in subparagraph (d) of this paragraph;
b) the '192 patent also fails to disclose supervisory layer software being integrated into a single DSP. At col. 3, line 9-et seq., the' 192 patent discloses a single integrated circuit chip for interfacing device control circuitry (which may contain a DSP) to a client machine via a computer network. The single integrated chip of the '192 patent includes interfaces for communicating with device control circuitry and with a computer network. Unlike the single chip of '192 patent, however, Claim 15 recites these and additional supervisory functions being run from a supervisory layer software in the DSP. As known to those skilled in the art, and as disclosed in the '192 patent, supervisory layer software functions are conventionally found on the application layer, and not on a DSP. ***However***, each DSP is not just hardware but contains therein software and such software was the claimed supervisory functions; which , as indicated, was anticipated to be integrated when taking advantage of the integration technology provided by the art;

c) the single chip of the '192 patent fails to disclose the supervisory functions of converting data communicated between the DSP and a device into a message for exchanging with a remote system; generating outgoing calls from the DSP to an internet service provider (ISP), and confirming whether a datum has been sent to a remote system. The DSP as recited in Claim 15 is sharply contrasted to single chip of the ' 192 patent since it comprises a memory in which is loaded an Internet protocol array, a signal processing program, and supervisory layer software. The '192 patent does not explicitly or implicitly disclose a DSP comprising such programs. The DSP of the '192 patent discloses in column 6, line 21 is in the device control circuitry 38, and does not comprise a memory in which is loaded an Internet protocol array or a supervisory layer software. ***However***, as indicate above, each DSP is not just hardware but contains therein software for contacting an Internet Service Provide and for error correction and prevention (i.e., checking datum has been sent as is the case in TCP/IP) and such software was the claimed supervisory functions and programs loaded into the memory of the DSP. Again, as indicated in subparagraph (a) above and in subparagraph (b) below of this paragraph, integration was a matter of system construction and when the whole of '192 is viewed on a single integrated monolithic chip, such supervisory software and programs would have been anticipated as stored in the memory(ies) of a chip;

d) the Applicant respectfully submits that there is utterly no teaching or suggestion for one skilled in the art to modify the '192 patent and to integrate the whole of the circuitry of Fig. 1(b), the network interface functionalities, and the supervisory functionalities into a single DSP, as recited in Claim 15. Also, the applicant notes that in view of the '192 patent there is no teaching or suggestion to reduce chip count, pin I/O and/or size. In fact, the '192 patent teaches a single web interfacing chip and, accordingly, nothing in the '192 patent teaches or suggests that data processing functionalities and/or supervisory functionalities can be integrated into such a chip. ***However***, as indicated in examiner's prior Office Action, it would have been obvious to those skilled in the data processing art to integrate the whole of the circuitries of figure 1B into a single integrated monolithic chip because such would reduce chip count, pin I/O, and size for the same reasons Personal Computers do not take up the area of a 10 story buildings or several city blocks as indicated at the end of this subparagraph. Furthermore, it would have been obvious to incorporate the network interface chip into such devices as a radio based cell phone per in col. 6 (line 1-et seq.) and thus clearly obvious to integrate the whole of all circuitry onto on a single chip for a single board within the cell phone. That is, per figure 1B, the device 34 being a cell phone could have all of its circuitry 38 and/plus network interface 36 placed/built onto one single monolithic integrated circuit chip because such would reduce chip count, pin I/O, and overall size. Integrating known circuitries is not novel and does not comprise a step towards an invention. Just because something has not been done, does not mean it was not obvious. The purpose of integration is to reduce chip count, thus reducing power consummation and pin I/O. Integration is not a matter of a novel and non-obvious invention but rather a packing function. The applicant's invention is not the integration of a monolithic chip, else there would be method claims as to how such a chip was fabricated, rather the invention is directed to several components and functions that are packaged into a single integrated circuit chip. Also, since '192 taught integrating Internet functions into at least one chip, it would have been obvious to integrate such functions included with, or alone, into the DSP of '192. Thus integration would have been obvious to those skilled in the art as of at least pre-1998. Per 206 USPQ 499 (Mattel,

Inc. v. Hyatt et al.) U.S. District Court Central District of California (Nos. 78-4232 and 78-4233) decided October 31, 1979:

i) "14.15 A comprehensive survey of voice response from computers is set forth in the proceedings of the International Conference on Communications of 1970 in an article entitled 'Prospectives in Voice Response from Computers' by William D. Chapman, Ex. 111. Chapman discusses the impact of integrated circuit technologies and states that current advances in largescale integration and in monolithic memories afford low cost storage of vast quantities of speech data. Essentially, in 1970, Chapman, as one of those skilled in the art, foresaw the use of monolithic memories as speech or sound information storage devices for use in a computerized system for recreating speech."

ii) "15.12 Monolithic technology, the process whereby electronic circuitry is so integrated and reduced in size that most or all of the components of a computer may be placed on a single 'chip', has led to a reduction of size and cost of computers. This technology existed in the prior art well before the date of the filing for the '540 patent and Hyatt's alleged invention."

ii) 15.13 Certain prior art dating before 1971 does not show monolithic technology. Other art, however, specifically shows the use of monolithic technology for computers. For example, Rice, 'LSI and Computer System Architecture', Computer Design (December 1970), Ex. 93, Rice 'Integration Between LSI and Computer System Architecture', Parallel Processor Systems, Technologies, and Applications (L.C. Hobbs et al. eds. 1970), Ex. 94, Hudson 'The Applications and Implications of Large Scale Integration', Computer Design (June 1968), Ex. 74, and other references demonstrate that monolithic technology and integrated circuit technology as the form of implementation for computer elements predated Hyatt's claimed invention. The specific application of monolithic technology to computerized sound generation is expressly discussed by Chapman and is implicit in Hovik. Furthermore, the claims in Hyatt's patent do not contain any qualification as to size, and many of the prior art methods for computerized generation of sound require no more computational power and no greater memory size than is required by Hyatt in his specifications. Thus, Hyatt attempted to characterize Booth and Booth as requiring 'quite a substantial amount of storage' and Hovik as requiring 'tens of thousands of samples,' 'if he wanted . . . a five-second tone, he would need 150,000 numbers stored in that ROM.' These characterizations are wholly inaccurate. Hovik, for example shows in figure 6 a highly complex waveform (much more complex than Hyatt illustrates). It is stored, in Hovik's system, as only sixteen eight-bit words and one MSB address location: 'As long as this waveform is desired (the 8 MSB's of the ROM address remain the same) the clock and counter providing the LSB address will cause continuous repetition of the analog waveform.'"

11. ***Claims 15-21 and 23-26 are rejected under 35 U.S.C. 103 (a)*** as being anticipated by Stern et al. (PCT WO 98/47252 art of record as provided by the applicant 21 November 2001).

12. Prior to addressing the claims, Stern et al details his DSP/RISC (11), in figure 1, as being a RS31100 chip (shown on pages 25/1 to 25/5) on pages 17 (line 29) to page 18 (line 28). By definition, in part, a DSP is one that can perform modem routines (see page 18 (line 1)), voice functions (page 18 (lines 2)), and/or fax functions (page 18 (line 13)). Stern also taught such software functions per the figure on page 25/10 as covered on page 18 (line 29-et seq.). By inspection of the figure on page 25/5 (marked as figure 2) the system functions on page 25/10

was implemented with/for the chip RS3110 per figure 1, of the figures in Stern, with software as covered in the figure of page 25/10 which there is shown also modem hardware and software functions (top center), sound and voice functions (center), fax functions (right lower). As indicated above, it would have been obvious to those skilled in the data processing art to integrate the whole of figure 2 (page 25/5) with the functions of the figure on page 25/10-et al. since portions of the functions (fax, modem, sound, voice, and the like) were already integrated into the DSP RS3110 specifically, per page 17-et seq., several of the functions were already integrated into the DSP per page 18 (lines 7-et seq.). Since the DSP had some functions (fax, modem, voice, exc.) of that of the figure on page 25/10, integrating more of the functions in the figure of 25/10 into the DSP would have been obvious because some of the functions had already been integrated into the DSP.

13. Per claim 15, when viewing figure 2 on page 10/5 as a single integrated monolithic chip with the functions of page 25/10-et seq., Stern et al. (herein Stern) taught an electronic component (e.g., see figure on page 25/10) and pages 17 (line 29) et seq.) for connecting to and exchanging data with a telecommunication network (e.g., see figure 1 of Stern), the electronic component comprising a DSP (Digital Signal processor) (e.g., see figure 1 (17) and paragraph 13 above) which DSP further comprised:
a) at least one memory in which is loaded a program for implementing the an Internet protocol array and for running at least one of a message handling routine, a FTP download routine and a routine providing Web server functionalities (e.g., see figure on page 25/10 (very top right)),
b) a signal processing program for exchanging data on the a telecommunications network (e.g., see figure on page 25/10 (XYZ modem (top center)), and,
c) a supervisory layer software (e.g., EROS starting with page 25/8-et seq) for converting data exchanged between the DSP and a communications device into data messages exchanged with a remote system and automatically generating outgoing calls to an internet service provider (ISP) and confirming whether a datum has been sent to the remote system;
d) wherein the protocol array, the signal processing program, and the supervisory layer software could obviously be jointly integrated in the DSP since the DSP (11) already contained several of the fax, modem, voice, functions of EROS and because of the advantages outline in subparagraph (d) above in 206 USPQ 499 (Mattel, Inc. v. Hyatt et al.) U.S. District Court Central District of California (Nos. 78-4232 and 78-4233) decided October 31, 1979.

14. Per claim 16, claim 17, claim 18, claim 19, and claim 20, as indicated above, Stern taught each a modem and telecommunications which encompassed all known telecommunications including, since not specifically excluded by Stern, electric radio network(s) (i.e., cell phones and standard land lines), page 7 (line 29), and page 18 (line 32) for analogue/digital conversion component.

15. Per claim 21 and claim 23, see the figure on page 25/5 (16 Megs of ROM and 16 megs of RAM) which was at least 8 kilowords and more for use in a communications device.

16. Per claim 24 and claim 25, call back is a standard function on busy signals to an ISP (ie., repeated dialing till through) where as NAT and DHCP are standard Internet functions as suggested by FTP, HTTP, SMTP, TCP/IP, exc... in the figure of 25/10.

17. Per claim 26, this claim does not teach or defined above the correspondingly rejected claims given above, and is thus rejected for the same reasons given above and additional elements such as being in a calculator, computer are calculators, keyboard, display (i.e., LCD) and the like are also shown in the figure of pages 25/5 and 25/10.

18. In summary, with respect to each of the applied references as substantial evidence of record and per the reasons of the Court(s), integrating the elements of the applied evidence of record (applied references), it would have been either an anticipated matter of packaging the system and/or a matter of obvious design choice to integrate these components as outlined above. Thus, for example, integrating the hardware and software of the figure on page 25/5 into a single integrated monolithic chip would have been obvious to those skilled in the art for the benefits as indicated in the citation(s) to 206 USPQ 499 (Mattel, Inc. v. Hyatt et al.) U.S. District Court Central District of California (Nos. 78-4232 and 78-4233) decided October 31, 1979. in conclusion, it would have been obvious to integrate either '192 and/or figure 2 on page 25.5 of Stern.

19. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert B. Harrell whose telephone number is (571) 272-3895. The examiner can normally be reached Monday thru Friday from 5:30 am to 2:00 pm and on weekends from 6:00 am to 12 noon Eastern Standard Time.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew T. Caldwell, can be reached on (571) 272-3868. The fax phone number for all papers is (703) 872-9306.

23. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

ROBERT B. HARRELL
PRIMARY EXAMINER
GROUP 2142